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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/039,656	12/31/2001	David L. Hill	042390.P13635	9210

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EXAMINER	
LI, ZHUO H	

ART UNIT	PAPER NUMBER
2185	

DATE MAILED: 12/15/2005

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/039,656	HILL ET AL.	
	Examiner	Art Unit	
	Zhuo H. Li	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-12,15-21,24-28 and 30* is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☒ Claim(s) *13-14, 22-23 and 29* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 December 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *See action please*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The Information Disclosures Statements filed on August 6, 2002, March 20, 2003, August 12, 2003, June 17, 2004, and February 18, 2005 have been considered.

Specification

2. The disclosure is objected to because of the following informalities:

Page 1, under title of Related Applications (lines 6-11), Applicants are required to list all the co-related applications' serial number and its corrected title.

Appropriate correction is required.

Drawings

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description:

Page 7, paragraph [0021] of the specification refers to "instruction pointers (170)" is not found in Fig. 1.

Page 7, paragraph [0023] of the specification refers to "replicated state (180)" is not found in Fig. 1.

Page 12, paragraph [0036] of the speciation refers to "bus controller (340)" is not found in Fig. 1.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claim 30 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. More specifically, the examiner has been unable to locate any particular structure(s) in the specification that discloses a partitioning and annealing logic to relinquish and/or re-partitioning of resources. And, one of ordinary skill in the art would not necessarily know what type of structure is capable of relinquishing/re-partitioning resources. If applicants believe it does

disclosed in at the time the application was filed, please point it out to the examiner with the detail page and line number in the response.

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 4-6 and 16 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 4 and 16, the phrase "any" renders the claim indefinite because it contains one, some, or all indiscriminately number or amount and unlimited or unmeasured quantity.

Claims 5-6 are also rejected because of depending on claim 4, containing the same deficiency.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claims 1-12, 15-21, and 24-28 are rejected under 35 U.S.C. 102(e) as being anticipated by Vartti (US PAT. 6,625,698).

Regarding claim 1, Vartti discloses a processor (200, figure 2) comprising a cache, i.e., second level cache (206, figure 2), an execution unit, instruction processor (202, figure 2) to execute an instruction having an operand indication a monitor address, i.e., requested address stored in the targeted storage unit, a bus controller, i.e., storage controller (204, figure 2) to assert a preventative signal, i.e., lock request, in response to receiving a memory access attempting to gain sufficient ownership, i.e., exclusive ownership, of a cache line associated with the requested address to allow a modification of the cache line without generation of another transaction indicative of the modification (figures 3-4 and col. 9 line 7 through col. 11 line 23).

Regarding claim 2, Vartti discloses the processor wherein the cache is an L1 cache (col. 4 line 63 through col. 5 line 7, and lines 38-55), and wherein the processor further comprises an L2 cache (206, figure 2).

Regarding claim 3, Vartti discloses the cache line associated with the monitor address is flushed from the L1 cache and the L2 cache in response to the instruction (col. 6 line 61 through col. 7 line 6).

Regarding claim 4, Vartti discloses the processor wherein the bus controller, i.e., storage controller, is to generate a bus cycle, make a request, in response to the instruction, the bus cycle to eliminate any ownership of the cache line by another processor that would allow modification of the cache line without generation of another transaction indicative of modification of the cache line (col. 6 lines 40-60, col. 7 line 53 through col. 8 line 18 and figures 3-4).

Regarding claim 5, Vartti discloses the bus cycle is a read and/or invalidating bus cycle (col. 7 line 53 through col. 8 line 18).

Regarding claim 6, Vartti discloses the processor further comprising a monitor, i.e., input logic (220, figure 2) coupled to the bus controller to monitor bus transactions for a transaction indicative of a write to the monitor address, and to signal a monitor event in response to the transaction indicative of the write to the monitor address (col. 5 line 66 through col. 6 line 18).

Regarding claim 7, Vartti discloses the processor further comprising a plurality of write combining buffers, i.e., memory register, between caches, a snoop port for the plurality of write combining buffers, a monitor coupled to the L1 cache and coupled to the snoop port to monitor memory access cycles from the execution unit and from the snoop port (col. 9 line 7 through col. 11 line 23).

Regarding claim 8, Vartti discloses an apparatus (100, figure 1) comprising a bus controller, i.e., input/output module (130, figure 1), having a plurality of bus cycle information line as defined in figure 1, a programmable memory access detection logic (110, figure 1) coupled to a bus, the programmable memory access detection logic comprising a storage location to store a monitor address specified by an instruction and comprising a storage location (206, figure 2) to store a monitor address, i.e., requested address, specified by an instruction, i.e., requesting instruction from instruction processor (202, figure 2), and comparison logic, i.e., storage controller (204, figure 2) having inputs (220, figure 2) coupled to the storage location, and the plurality of bus cycle information lines, and a comparison logic output, i.e., bus control (224 and 226, figure 2) and (col. 5 line 66 through col. 6 line 18), coherence logic, i.e., control logic (216, figure 2) coupled to receive the monitor address, that in response to the instruction is

generate a read and/or invalidate transaction for a cache line associated with the monitor address (col. 5 lines 56-65).

Regarding claim 9, Vartti discloses the programmable memory access detection logic comprises write detection logic (220, figure 2).

Regarding claim 10, Vartti discloses the apparatus further comprising hit generation logic (218, figure 2) coupled to the storage location and the bus controller, wherein the hit generation logic has an output hit signal externally available to couple to a system bus (figure 2 and col. 5 lines 56-64).

Regarding claim 11, Vartti discloses the bus controller is to generate, in response to the instruction, a bus cycle chosen from a set consisting of a bus read/write lines invalidate of the cache line associated with the monitor address (col. 7 line 52 through col. 8 line 29).

Regarding claim 12, Vartti discloses the read and/or invalidate transaction is to ensure that no other processor caches include the cache line associated with the monitor address in a modified or exclusive state (col. 6 lines 40-60, col. 8 lines 19-60, and col. 9 line 7 through col. 11 line 23).

Regarding claim 15, Vartti discloses a method comprising performing a first bus transaction to eliminate ownership by other agents of a cache line associated with a monitor address i.e., requested address, specified by an instruction, i.e., requesting instruction from instruction processor (202, figure 2), asserting a preventative signal, i.e., lock requested, in response to a second bus transaction, i.e., other processor requested, attempting to gain ownership of the cache line associated with the monitor address (col. 9 line 7 through col. 11 line 23 and figures 3-4).

Regarding claim 16, Vartti discloses the first bus transaction comprises preventing any system processor cache from storing the cache line associated with the monitor address in a modified or exclusive state (col. 9 line 7 through col. 11 line 23, and figures 3-4).

Regarding claims 17-18, Vartti discloses the method wherein the fist bus transaction comprises performing an invalidating transaction and a read transaction (col. 8 line 10 through col. 9 line 6).

Regarding claim 19, Vartti discloses the method wherein asserting the preventative signal, i.e., lock signal, comprises asserting a hit signal in response to a transaction which could result in a bus agent gaining ownership of the cache line associated with the monitor address, i.e., requested address, (col. 9 line 7 through col. 11 line 23 and figures 3-4).

Regarding claim 20, Vartti discloses the monitor address is an operand of the instruction (col. 2 lines 11-21 and col. 3 lines 52-62).

Regarding claim 21, Vartti discloses flushing the cache line from a plurality of processor caches in a processor that executes the instruction (col. 6 line 61 through col. 7 line 6).

Regarding claim 24, the limitations of the claim are rejected as the same reasons set forth in claim 8.

Regarding claim 25, Vartti discloses hit generation logic (216, figure 2) to generate a hit signal in response to a read transaction to the cache line associated with the monitor address (col. 5 lines 56-65).

Regarding claim 26, the limitations of the claim are rejected as the same reasons set forth in claim 21.

Regarding claims 27-28, the limitations of the claims are rejected as the same reasons set forth in claims 15-18.

Allowable Subject Matter

10. Claims 13-14, 22-23 and 29 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

11. Claim 30 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, First paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Emer et al. (US PAT. 6,493,741) discloses method and apparatus to quiesce a portion of a simultaneous multithreaded central processing unit (abstract).

Kalafatis et al. (US PAT. 6,535,905) discloses method and apparatus for thread switching within a multithreaded processor (abstract).

Rajwar et al (US Pub No. 2003/0,079,094) discloses concurrent execution of critical sections by eliding ownership of locks in a multi-threaded programs (abstract).

Boatright ea al. (US PAT. 6,463,511) discloses system and method for high performance execution of locked memory instructions in a system with distributed memory and a restrictive memory model (abstract).

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zhuo H. Li whose telephone number is 571-272-4183. The examiner can normally be reached on Tues - Fri 9:00am - 6:30pm and alternate Monday..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

14. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

BEHZAD JAMES PEIKARI
PRIMARY EXAMINER

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Art Unit 2185